REMARKS

By the present amendment and response, independent claims 20 and 21 have been amended to overcome the Examiner's objections and claims 22-28 have been added. New claim 22 is the independent form of claim 2, which includes all of the limitations of base claim 20. New claims 23-28 depend from claim 22 and correspond to dependent claims 3 and 5-9, respectively. New claims 22-28 are thus allowable according to the Examiner's comments on page 4 of the Office Action dated December 30, 2002. Thus, claims 2-9, 11-13, and 20-28 remain in the present application and claims 22-28 are now in condition for allowance. Reconsideration and allowance of outstanding claims 2-9, 11-13, and 20-21 in view of the claim amendments and the following remarks are requested.

The Examiner has rejected claims 4 and 20 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,373,114 to Jeng et al. ("Jeng"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 20, is patentably distinguishable over Jeng.

The present invention, as defined by amended independent claim 20, teaches, among other things, "a diffusion barrier layer directly overlying the dielectric layer, said diffusion barrier layer being a single layer" and "a gate electrode directly overlying the diffusion barrier layer, said gate electrode layer comprising a semiconductor material." As disclosed in the present application, utilizing silicon germanium, i.e. a semiconductor material, in a gate of a device may lower the temperature at which the device is annealed

to activate dopants in a channel region. By lowering the processing temperature, an undesirable interfacial layer that can form between the dielectric layer and the channel region at high annealing temperatures can be reduced or eliminated. As a result, the present invention advantageously achieves reduced leakage current in the channel and increased device operating speed.

Additionally, as disclosed in the present application, by utilizing a diffusion barrier layer directly between the dielectric layer and the gate electrode, the present invention advantageously prevents a dopant, such as germanium, in the gate electrode from contaminating the dielectric layer during thermal cycling. Furthermore, by utilizing a single diffusion barrier layer, the present invention advantageously achieves prevention of dielectric layer contamination without incurring the additional processing cost of multiple protective layers situated between the gate electrode and gate dielectric layer.

In contrast to the present invention as defined by amended independent claim 20, Jeng does not teach, disclose, or suggest "a diffusion barrier layer directly overlying the dielectric layer, said diffusion barrier layer being a single layer" and "a gate electrode directly overlying the diffusion barrier layer, said gate electrode layer comprising a semiconductor material." Jeng specifically discloses partial silicon layer 56, which is formed over gate dielectric layer 54, and barrier film 58, which is formed over partial silicon layer 56 and which can be considered a second silicon layer. See, for example, Jeng, column 4, lines 23-43. In Jeng, metallic layer 60, which can comprise any of a

number of highly conductive materials containing metal, is formed over barrier film 58. See, for example, Jeng, column 5, lines 45-48. In Jeng, two silicon layers, i.e. barrier film 58 and partial silicon layer 56, are situated between metallic layer 60 and gate dielectric layer 54 and utilized to prevent contaminate diffusion from reaching gate dielectric layer 54. Furthermore, Jeng requires metallic layer 60 to comprise a highly conductive material containing metal. For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 20, is not suggested, disclosed, or taught by Jeng. As such, amended independent claim 20 is patentably distinguishable over Jeng. Thus claims 2-9 depending from amended independent claim 20 are also patentably distinguishable over Jeng for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 11-13 and 21 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,353,249 to Boyd et al. ("Boyd"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 21, is patentably distinguishable over Boyd.

The present invention, as defined by amended independent claim 21, teaches, among other things, "a well, said well comprising two silicon germanium filled spaces," "wherein said two silicon germanium filled spaces comprise respective source/drain regions of second conductivity type, said respective source/drain regions being situated on opposite sides of the channel region." As disclosed in the present application, portions

of a well are removed and spaces left by the removed portions of the well are filled with silicon germanium to form source/drain regions, which are then doped. The portions of the well can be removed by, for example, etching away portions of the well. By forming source/drain regions by removing portions of the well, the present invention can advantageously control the size of the source/drain regions by controlling the quantity of material that is removed from the well. Additionally, by filling removed portions of the well with silicon germanium to form source/drain regions, the present invention advantageously achieves source/drain regions that can comprise a different material than the well. Furthermore, by utilizing silicon germanium to form source/drain regions, the present invention advantageously achieves a device that allows a lower annealing temperature to be utilized to active dopants in the channel region so as to prevent diffusion between the source/drain regions from destroying the channel.

In contrast to the present invention as defined by amended independent claim 21, Boyd does not teach, disclose, or suggest "a well, said well comprising two silicon germanium filled spaces," "wherein said two silicon germanium filled spaces comprise respective source/drain regions of second conductivity type, said respective source/drain regions being situated on opposite sides of the channel region." Boyd specifically discloses utilizing conventional ion implantation and annealing to form source/drain regions 32. See, for example, column 7, lines 16-19 and Figure 1G of Boyd. Thus, Boyd does not teach, disclose, or suggest filling spaces in a well with silicon germanium to

form source/drain regions. In fact, Boyd does not even disclose a well in which to form source/drain regions. For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 21, is not suggested, disclosed, or taught by Boyd. As such, amended independent claim 21 is patentably distinguishable over Boyd. Thus claims 11-13 depending from amended independent claim 21 are also patentably distinguishable over Boyd for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 20 and 21, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 2-9, 11-13, and 20-21 are patentably distinguishable over the art cited by the Examiner. For all the foregoing reasons, an early allowance of claims 2-9, 11-13, and 20-21 and an early Notice of Allowance for all pending claims 2-9, 11-13, and 20-28 is respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 3/3/03

Michael Farjami, Esq.
Reg. No. 38, 135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Telephone: (949) 784-4600
Facsimile: (949) 784-4601

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner of Patents and Trademarks; Washington, D.C. 20231

Date of Deposit: 3/3/03

Lori Lhave
Name of Person Mailing Paper and/or Fee

Lori Lhave 3/3/03
Signature Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 20 and 21 have been amended as follows:

20. (Twice Amended) A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

a diffusion barrier layer directly overlying the dielectric layer, said diffusion barrier layer being a single layer;

a gate electrode directly overlying the diffusion barrier layer, said gate electrode layer comprising a semiconductor material;

a blocking layer overlying the gate electrode; and

two source/drain regions of second conductivity type formed on opposite sides of the channel region.

21. (Twice Amended) A semiconductor device formed on a substrate and comprising:

a well, said well comprising two silicon germanium filled spaces;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region; and

a gate electrode overlying the dielectric layer; [and]

wherein said two silicon germanium filled spaces comprise [two] respective source/drain regions of second conductivity type, said respective source/drain regions being situated [formed] on opposite sides of the channel region[, wherein the source/drain regions comprise silicon germanium].